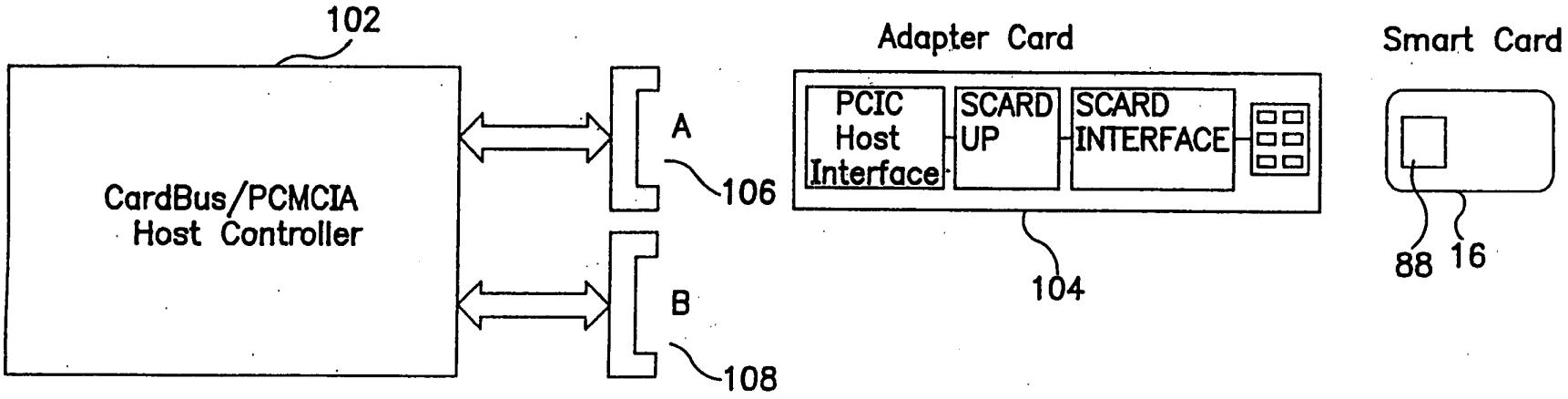
102
CardBus/PCMCIA
Host Controller
A
B
106
108
Adapter Card
PCIC
Host
Interface
SCARD
UP
SCARD
INTERFACE
104
Smart Card
88
16

FIG. 1

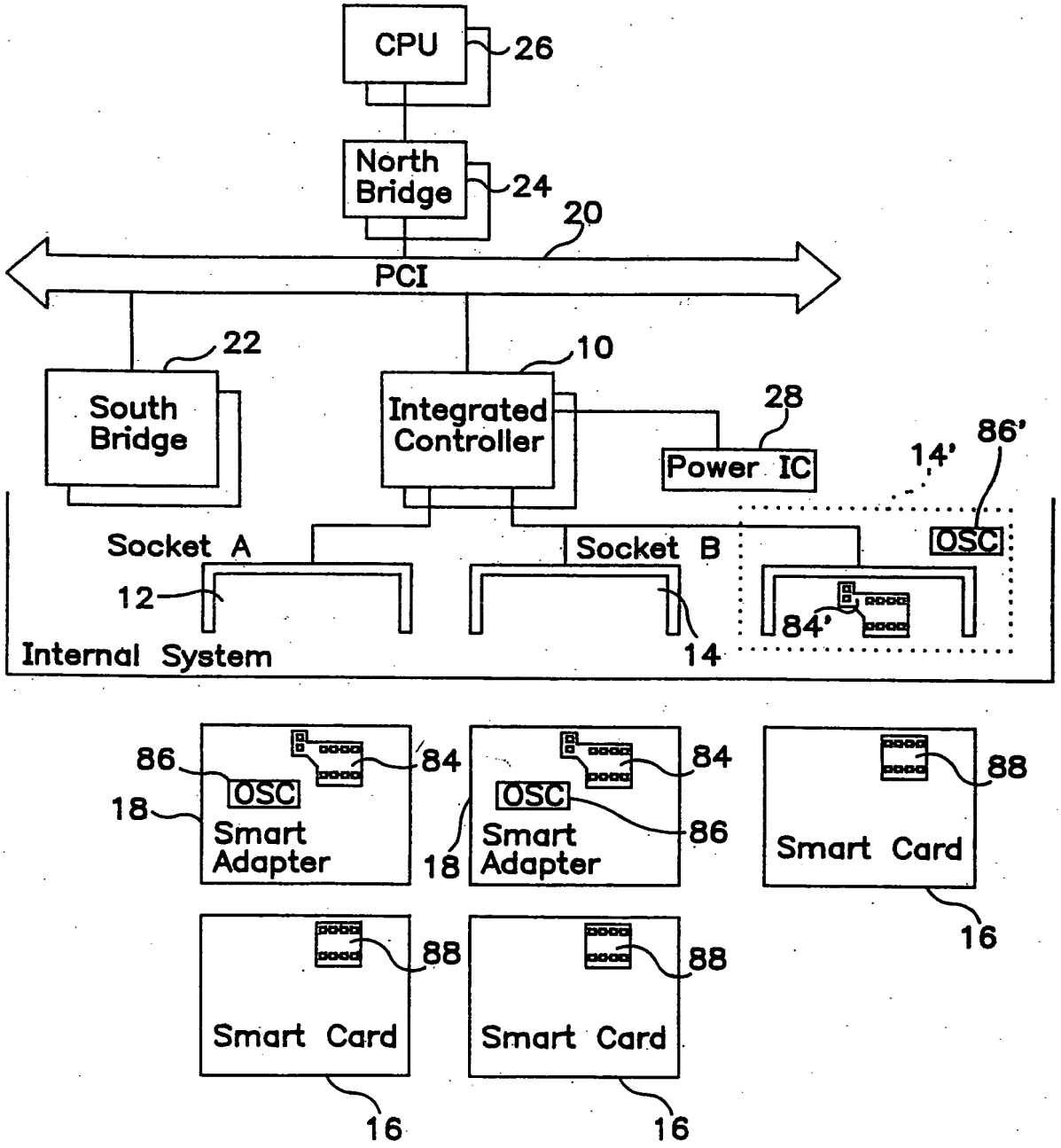
CPU
26
North Bridge
24
20
PCI
22
South Bridge
10
Integrated Controller
28
Power IC
14'
86'
OSC
Socket A
Socket B
12
84'
14
Internal System
86
84
OSC
18
Smart Adapter
84
OSC
86
18
Smart Adapter
88
Smart Card
16
88
Smart Card
16
88
Smart Card
16

FIG. 2

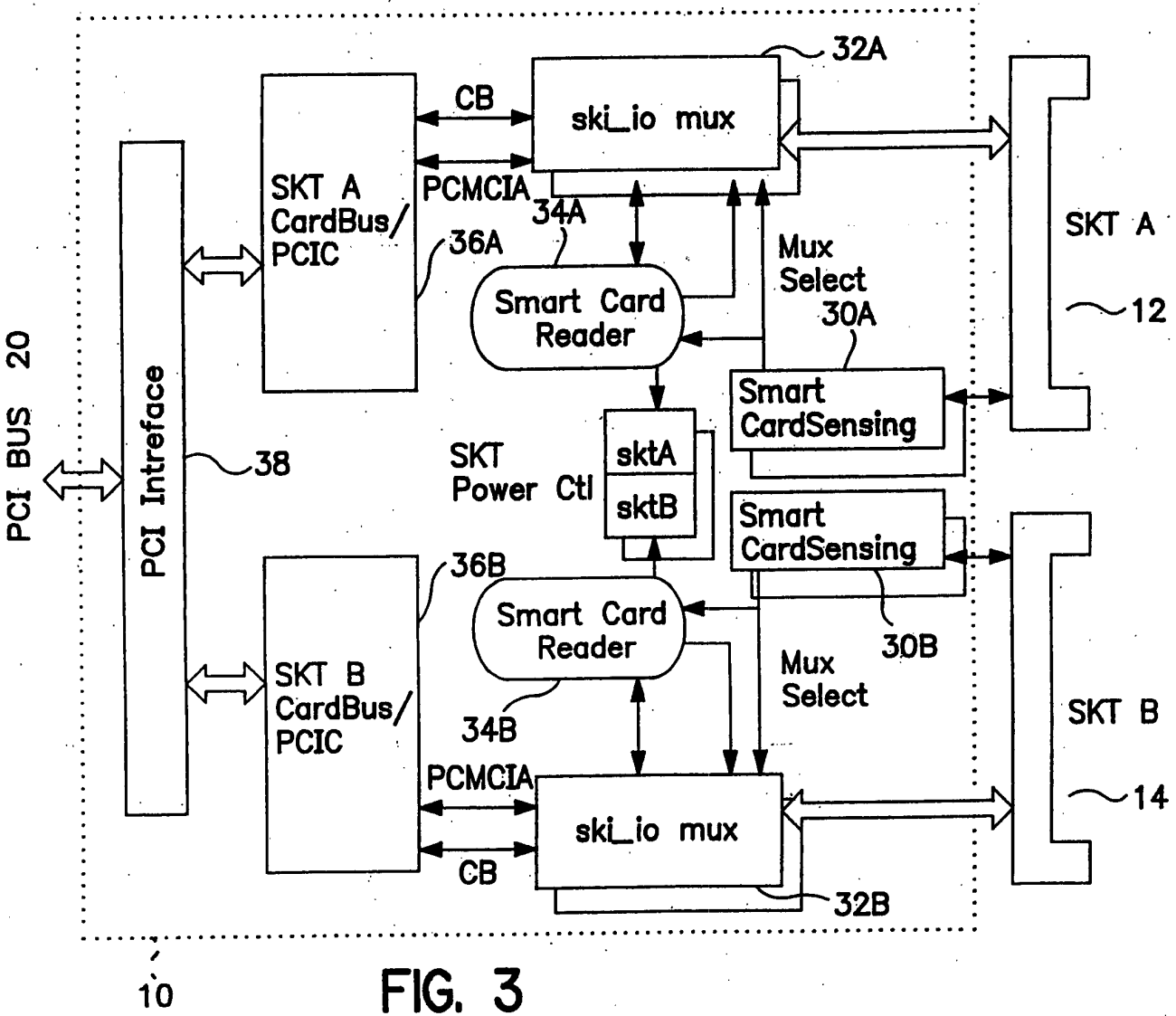
PCI BUS 20
PCI Intreface
38
SKT A
CardBus/
PCIC
SKT B
CardBus/
PCIC
CB
PCMCIA
ski_io mux
32A
34A
36A
Smart Card
Reader
Mux
Select
30A
Smart
CardSensing
SKT A
12
SKT
Power Ctl
sktA
sktB
36B
Smart Card
Reader
34B
Smart
CardSensing
30B
Mux
Select
SKT B
14
PCMCIA
CB
ski_io mux
32B
10

FIG. 3

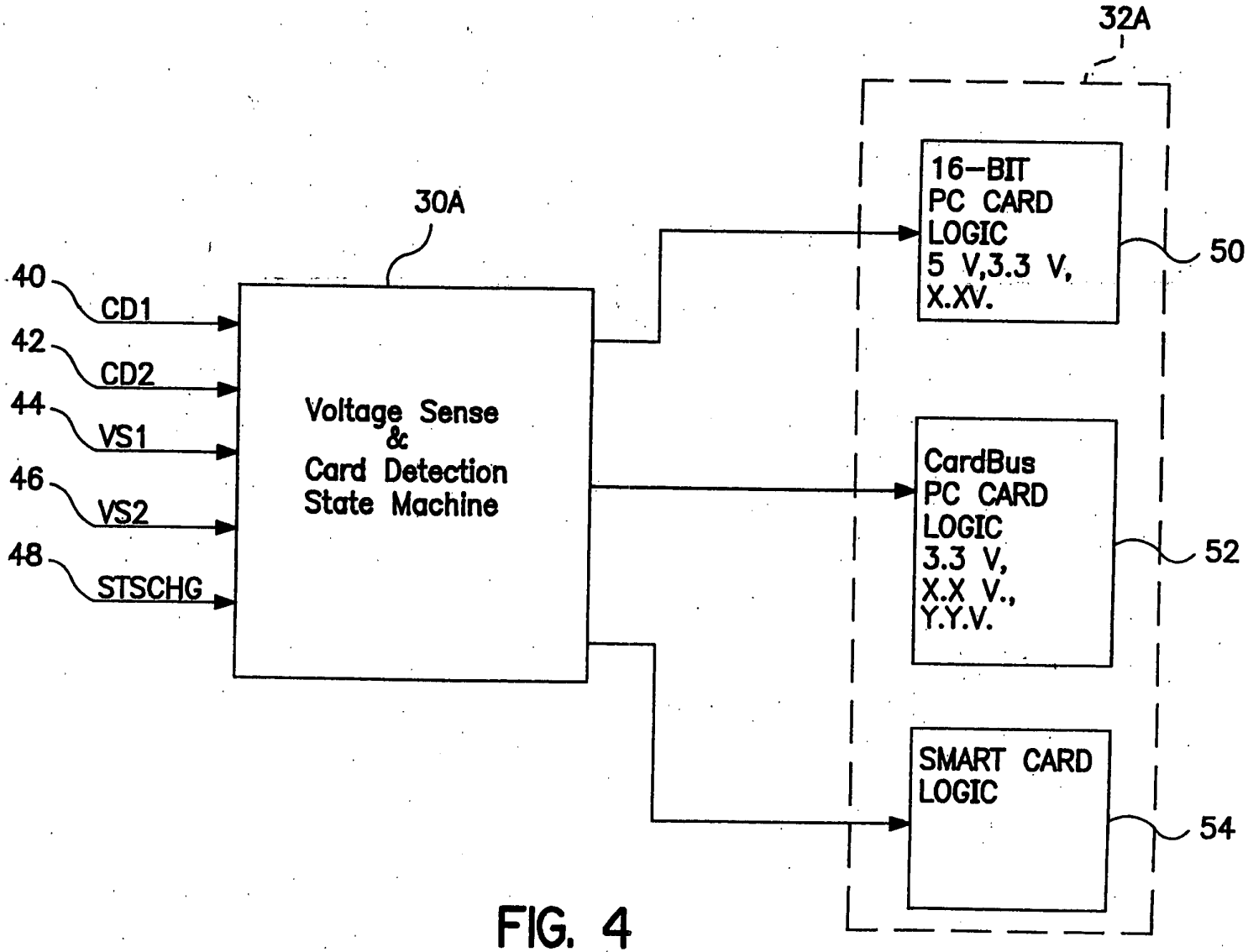
32A
30A
40
CD1
42
CD2
44
VS1
46
VS2
48
STSCHG
Voltage Sense
&
Card Detection
State Machine
16-BIT
PC CARD
LOGIC
5 V,3.3 V,
X.XV.
50
CardBus
PC CARD
LOGIC
3.3 V,
X.X V.,
Y.Y.V.
52
SMART CARD
LOGIC
54

FIG. 4

CD2#/CCD2# (pin 67)	CD1#/CCD1# (pin 36)	VS2#/CVS2 (pin 57)	VS1#/CVS1 (pin 43)	Card Type		
				Key	Interface	Voltage
ground	ground	open	open	5V	16-bit PC Card	5 V
ground	ground	open	ground	5V	16-bit PC Card	5 V and 3.3 V
ground	ground	ground	ground	5V	16-bit PC Card	5 V. 3.3 and X.XV
ground	ground	open	ground	LV	16-bit PC Card	3.3 V
ground	connect to CVS1	open	connect to CCD1#	LV	CardBus PC Card	3.3 V
ground	ground	ground	ground	LV	16-bit PC Card	3.3 V and X.X V
connect to CVS2	ground	connect to CCD2#	ground	LV	CardBus PC Card	3.3 V and X.X V
connect to CVS1	ground	ground	connect to CCD2#	LV	CardBus PC Card	3.3 V.X.X V and Y.Y V
ground	ground	ground	open	LV	16-bit PC Card	X.X V
connect to CVS2	ground	connect to CCD2#	open	LV	CardBus PC Card	X.X V
ground	connect to CVS2	connect to CCD1#	open	LV	CardBus PC Card	X.X V and Y.Y V
connect to CVS1	ground	open	connect to CCD2#	LV	CardBus PC Card	Y.Y V
ground	connect to CVS1	ground	connect to CCD1#	reserved		
ground	connect to CVS2	connect to CCD1#	ground	reserved		

FIG. 5

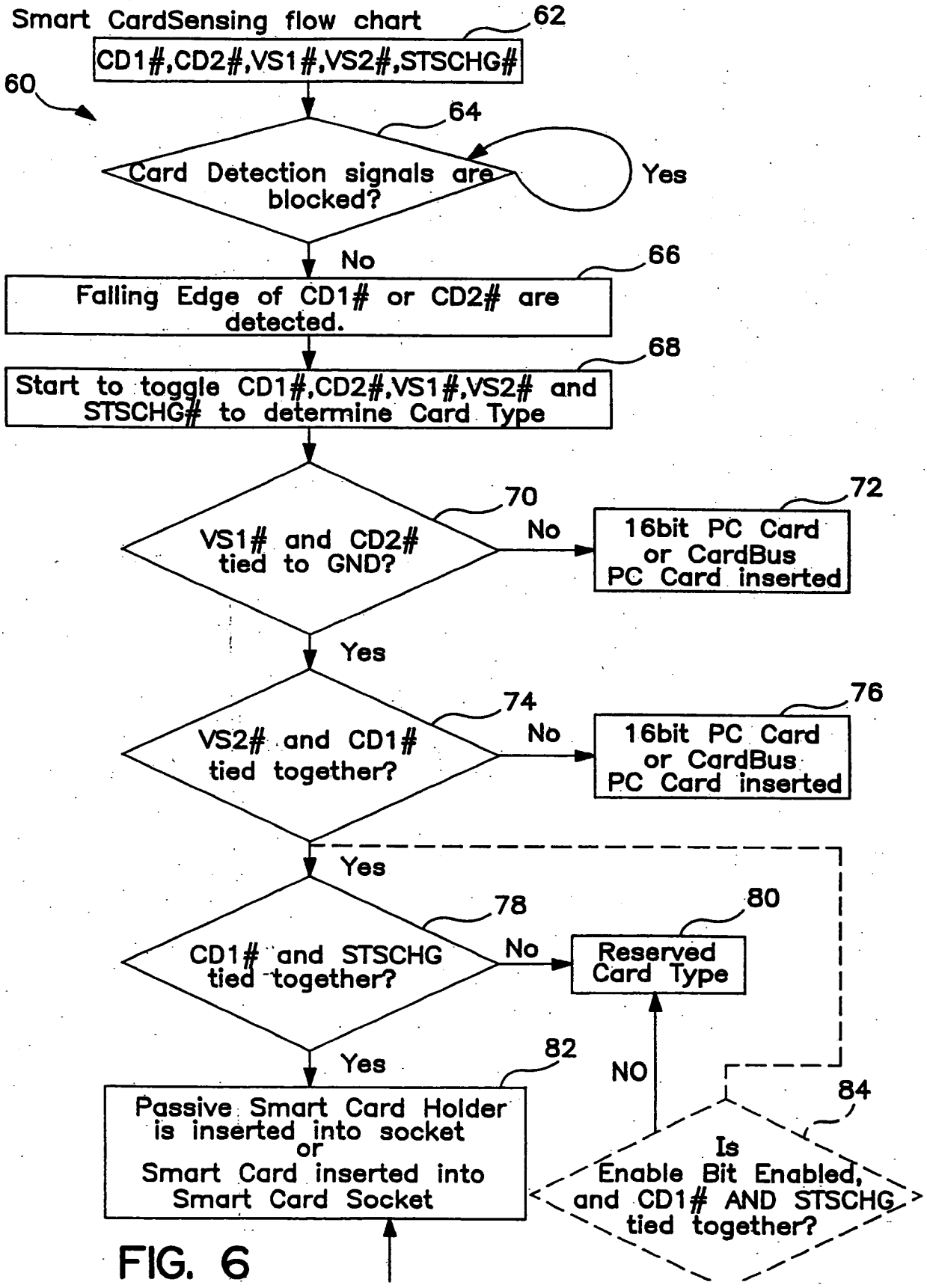
Smart CardSensing flow chart
62
CD1#,CD2#,VS1#,VS2#,STSCHG#
60
64
Card Detection signals are blocked?
Yes
No
66
Falling Edge of CD1# or CD2# are detected.
68
Start to toggle CD1#,CD2#,VS1#,VS2# and STSCHG# to determine Card Type
70
VS1# and CD2# tied to GND?
No
72
16bit PC Card or CardBus PC Card inserted
Yes
74
VS2# and CD1# tied together?
No
76
16bit PC Card or CardBus PC Card inserted
Yes
78
CD1# and STSCHG tied together?
No
80
Reserved Card Type
Yes
82
Passive Smart Card Holder is inserted into socket
or
Smart Card inserted into Smart Card Socket
NO
84
Is Enable Bit Enabled, and CD1# AND STSCHG tied together?

FIG. 6

Smart Card interface signals

PCMCIA PIN	Legacy Devices				Smart Card	
	16-bit PC Card		CardBus PC Card		Smart Card	
	Signal	I/O	Signal	I/O	Signal	I/O
17, 51	VCC		VCC		VCC	
58	RESET	O	CRST#	O	RESET	O
47	A18	O	Reserved		CLOCK	O
32	D2	I/O	Reserved		Rvd_C4	O
	GND		GND		GND	
18	VPP1		VPP1		VPP	
16	IREQ#	I	CINT#	I	I/O	I/O
40	D14	I/O	Reserved		Rvd_C8	O

FIG. 7A

Smart Card Detection signals

PCMCIA PIN						
	16-bit PC Card		CardBus PC Card		Smart Card	
	Signal	I/O	Signal	I/O	Signal	I/O
63	STSCHG#	I	CSTSCHG	I	Smart Card	I
36	CD1#	I	CCD1#	I	CD1#	I
43	VS1#	I	CVS1#	I/O	VS1#	I/O
57	VS2#	I	CVS2#	I/O	VS2#	I/O
67	CD2#	I	CCD2#	I	CD2#	I

FIG. 7B